Intel® 82805AA Memory Translator Hub (MTH)

Datasheet

November 1999

Order Number: 290632-001

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Revision History

Rev.	Draft/Changes	Date
-001	• Initial Release	November 1999

Intel® 82805AA MTH

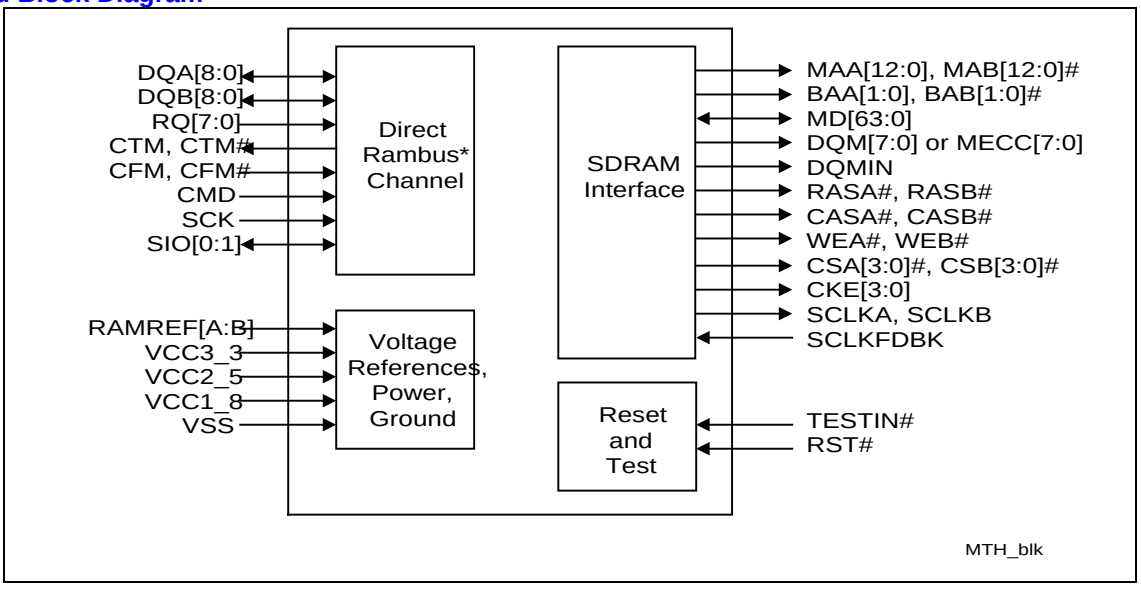
Product Features

- Write buffer to support modified Direct Rambus* write protocol
- Supports Powerdown and Self Refresh Low Power states of SDRAMs
- Clock generation for SDRAMs
- 1 cycle and 2 cycle rule supported
- Direct Rambus* channel Current Calibration, Temperature Calibration, and Levelization support
- Support of Direct Rambus* Channel CMOS signals to facilitate initialization and read/write of MTH registers
- 100 MHz SDRAMs on DIMMs
- 64Mbit and 128Mbit SDRAM technologies
- X4, x8, and x16 SDRAM components
- X4 Registered DIMMs
- 3.3V I/O for SDRAM
- 400 MHz Direct Rambus* Channel
- Maximum of 4 SDRAM rows per MTH. All rows share the same SDRAM data bus
- 241-pin mini-BGA

The Intel® 82805AA Memory Translator Hub (MTH) provides the capability to support SDRAM memory on a Direct Rambus* Channel. The MTH is designed for the Intel® 820 chipset platform. The MTH has a Direct Rambus* interface and a SDRAM interface. The MTH supports standard SDRAM DIMMs.

Each MTH can support up to 4 SDRAM rows. All four SDRAM rows from the MTH can be used to support up to 2 DIMMs. There are two rows per DIMM.

Simplified Block Diagram



The Intel® 82805AA Memory Translator Hub (MTH) may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

1. Overview

The Intel® 82805AA Memory Translator Hub (MTH) provides the capability to support SDRAM memory on a Direct Rambus* Channel. The MTH is intended to be used with the 82820 MCH and connects to the MCH's RDRAM channel. The MTH mode includes the following features:

- 64Mbit and 128Mbit SDRAM technologies
- 3.3V 100 MHz SDRAM (PC-100)
- x16, & x8 SDRAM configurations
- CBR refresh
- Clock Stop/Start support
- 400 MHz Rambus* channel support between MTH and MCH
- Utilizes Serial Presence Detection (SPD) for memory interface initialization

Terminology and Definitions

MCH	The Memory Controller Hub component that contains the processor interface, DRAM controller, and AGP interface. It communicates with the ICH over a proprietary interconnect called hub link.
Host	This term is used synonymously with processor.
Core	The internal base logic in the MTH.
RSL	Direct Rambus* Signaling Level is the name of the signaling technology used by Direct Rambus*.
RAC	Direct Rambus* ASIC Cell. It is the embedded cell designed by Rambus that interfaces with the Direct Rambus* devices using RSL signaling. The RAC communicates to the RMC.
RMC	Direct Rambus* Memory Controller. This is the logic that directly interfaces to the RAC.
RIMM	Direct Rambus* Inline Memory Module. RIMMs serve the same purpose as DIMMs except RIMMs contain Direct Rambus* devices while DIMMs contain SDRAM devices.
MCP	Memory Controller Packet. These packets contain the commands for the Direct Rambus* Channel. The packets initiate Direct Rambus* reads and writes.

1.1. Supported Memory Configurations

The Intel® 82820 MCH supports 64Mbit and 128Mbit SDRAM memory technologies with the following DRAM configurations. **Table 1** shows the memory configurations supported by the 82805AA MTH.

Table 1. SDRAM Configurations

Technology	Configuration	# of Row Address Bits	# of Col Addrs Bits	#of Bank Addrs Bits	Page Size
64 Mbit	8M x 8	12	9	2	4 KB
64 Mbit	4M x 16	12	8	2	2 KB
128 Mbit	32MX4	12	11	2	16 KB
128 Mbit	16M x 8	12	10	2	8 KB

NOTES:
1. 32MX4 128 Mbit support is for registered DIMMs only. 4MX16 64 Mbit support is for un-buffered DIMMs only.

1.1.1. Maximum Memory with DIMMs for PC Platforms

Table 2 shows the maximum memory for DIMM based platforms. See Figure 1 and Figure 2 for system layout and MTH on motherboard layout. The DIMM solution is implemented using a riser card with DIMM connectors.

Table 2. Maximum Memory Support for DIMM-based Platforms

DRAM Configuration		1 DIMM		2 DIMMs	
		SS	DS	SS	DS
64Mbit	8Mx8	64 MB	128 MB	128 MB	256 MB
64Mbit	4Mx16	32 MB	64 MB	64 MB	128 MB
128Mbit	16Mx8	128 MB	256 MB	256 MB	512 MB
128Mbit	32Mx4 Reg.	256 MB	512 MB	512 MB	1024 MB

NOTES:
1. Only two DIMM slots are on the motherboard
2. Single Sided DIMM uses one SDRAM row. (SS = Single Sides)
3. Double Sided DIMM uses two SDRAM row. (DS = Double Sides)
4. Maximum memory based on Intel® 82820 MCH implementation

Figure 1. MTH Supporting Un-buffered and Registered DIMMs on PC Systems

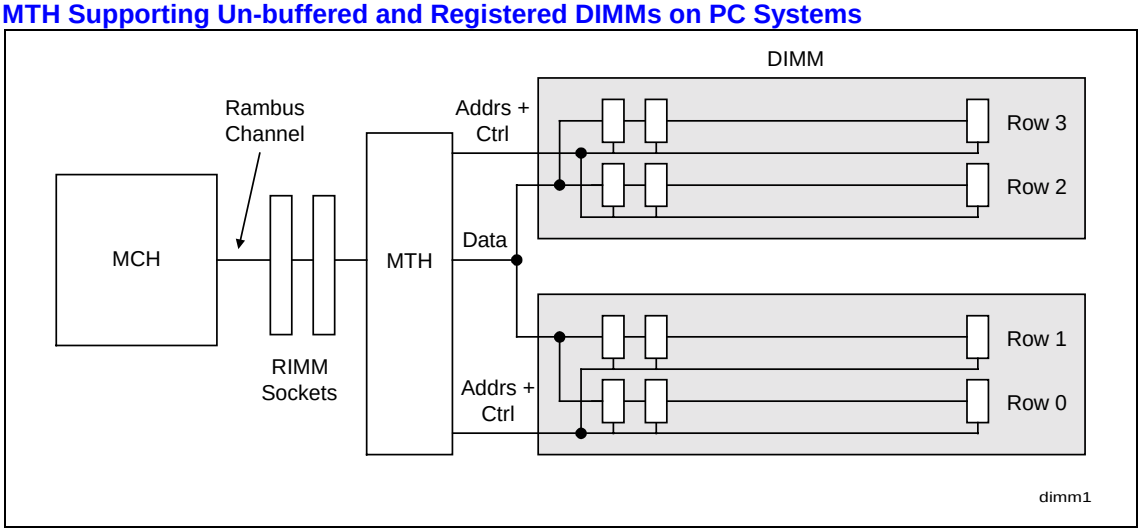
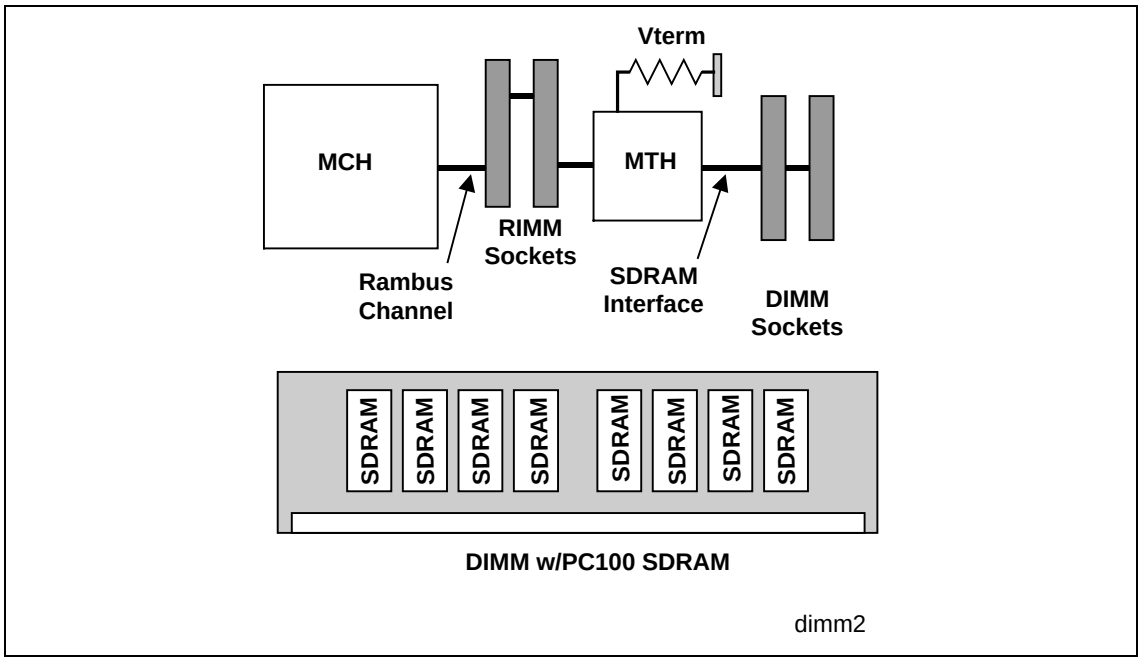


Figure 2. DIMM Connection



1.2. Direct Rambus* Channel Interface

The Direct Rambus* channel interface is the interconnection between the 82820 MCH and 82805AA MTH. The Direct Rambus* channel interface consists of 30 RSL signals (4 are clocks) and 3 CMOS signals. The MTH supports the following Direct Rambus* and SDRAM clock frequency combination. See **Table 3**.

Table 3. Frequency Configurations

Rambus* Frequency (MHz)	SDRAM Frequency (MHz)	Host Bus Frequency (MHz)
400	100	100
400	100	133

1.3. SDRAM Interface

The MTH supports up to four 64/72 bit wide rows of SDRAM. Two copies of MA, BA, RAS#, CAS# and WE# signals are provided. Also, 8 (two per row) copies of CS# and four copies (1 per row) of CKE signals are provided.

1.4. Clock Interface

The MTH provides two copies of SDRAM clock sources to be used with an external clock buffer for use with DIMMs. A clock feedback input is provided to phase align the MTH.

2. Signal Description

This chapter describes the MCH signals. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name the signal is asserted when at the high voltage level.

The following notations are used to describe the signal types and their drive state:

I Input pin

O Output pin

I/O Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

RSL Rambus* Signaling Level interface signal.

CMOS CMOS buffers.

The three CMOS signals mentioned in Table 4 support the following operations:

- Direct RDRAM device configuration
- SIO pin initialization
- SIO operations (includes accesses and device reset)
- Device selection for PowerDown exits

2.1. Direct Rambus* Channel

All signals are 2.5 volt except for Rambus* CMOS signals which are 1.8 volt.

Table 4. Direct Rambus* Channel Signals

Signal	Type	Description
DQA[8:0]	I /O RSL	**Data Bus (Data Byte A).** Bi-directional 9-bit data bus A. These signals correspond to the DQA [8:0] signals on the Direct Rambus* Channel.
DQB[8:0]	I/O RSL	**Data Bus (Data Byte B).** Bi-directional 9-bit data bus B. These signals correspond to the DQB [8:0] signals on the Direct Rambus* Channel.
RQ[7:0]	I RSL	**Request Control.** These signals carry the Memory Control Packets (MCP) from the MCH to the MTH. RQ[7:0] correspond to the RRq[2:0] and CRq[4:0] signals on the Direct Rambus* Channel respectively.
SIO0	I/O CMOS	**Serial IO Chain 0:** The serial input/output pin is used for reading and writing control registers. This corresponds to the SIO signal on the Direct Rambus* Channel.
SIO1	I/O CMOS	**Serial IO Chain 1:** This bi-directional signal is used to carry data for SIO operations, register access, MTH reset, and MTH ID initialization.
SCK	I CMOS	**Serial Clock:** Clock source used for timing of the SIO and CMD signals. This signal corresponds to the SCK signal on the Direct Rambus* Channel.
CMD	I CMOS	**Serial Command:** Serial command input used for control register read and write operations. This signal corresponds to the CMD signal on the Direct Rambus* Channel.
CTM	I RSL	**Clock To Master:** One of the two differential transmit clock signals used for MTH to MCH operations.
CTM#	I RSL	**Clock To Master Complement:** One of the two differential transmit clock signals used for MTH to MCH operations.
CFM	I RSL	**Clock From Master:** One of the differential receive clock signals used for MCH to MTH operations.
CFM#	I RSL	**Clock From Master Complement:** One of the differential receive clock signals used for MCH to MTH operations.

2.2. SDRAM Interface

Table 5. SDRAM Interface Signals (3.3V)

Signal	Type	Description
MAA[12:0], MAB[12#,11#, 10,9:0#]	O CMOS	**SDRAM Memory Address:** These signals provide multiplexed row and column addresses to SDRAM. There are two sets of MA signals (MAAx and MABx). Each set can drive up to two rows of SDRAM. MAB [12:11, 9:0] are inverted copies of MAA[12:11, 9:0]; MAA10 and MAB10 are identical copies.
BAA[1:0], BAB[1:0]#	O CMOS	**SDRAM Bank Address:** These signals provide bank address to SDRAM. There are two sets of BA signals (BAA and BAB). Each set can drive up to two rows of SDRAM. The BAB [1:0] are inverted copy of BAA[1:0].
MD[63:0]	I/O CMOS	**SDRAM Data:** MD[63:0] are the data bus signals for SDRAM.
DQM[7:0] or MECC[7:0]	O CMOS	**SDRAM Data Mask:** DQM[7:0] are available as SDRAM byte enables for write data in systems that do not support ECC. **Memory ECC Data:** MECC[7:0] provide ECC data during write operations in systems that support ECC. When ECC is supported, all writes are read-modify-writes; hence, the DQM signals of the SDRAM devices can be tied to logic zero.
DQMIN	O CMOS 3.3V	**DQM Input (SDRAM Input):** DQMIN is only used when the MTH is in ECC mode. When the MTH is in ECC mode, this signal must be connected to all DQM pins of the SDRAMs. After the power up of the MTH, DQMIN is driven high until the SDRAM initialization done (SID) bit in the MOR register is set to 1. When SID is 1, this signal is driven 0.
RASA#, RASB#	O CMOS	**SDRAM Row Address Strobe:** These signals are used to latch the row and bank addresses on the MAxx and BAxx lines into SDRAM. Each signal can drive up to two SDRAM rows.
CASA#, CASB#	O CMOS	**SDRAM Column Address Strobe:** These signals are used to latch the column and bank addresses on the MAxx and BAxx lines into SDRAM. Each signal can drive up to two SDRAM rows.
WEA#, WEB#	O CMOS	**SDRAM Write Enable:** These signals are used for write and pre-charge operations of SDRAM. Each signal can drive up to two SDRAM rows.
CSA[3:0]#, CSB[3:0]#	O CMOS	**SDRAM Chip Select:** These signals are used for selecting the SDRAM row . There are two copies for each SDRAM row (CSAx# is a copy of CSBx#). CSA0# and CSB0# activate SDRAM row 0. CSA1# and CSB1# activate SDRAM row 1. CSA2# and CSB2# activate SDRAM row 2. CSA3# and CSB3# activate SDRAM row 3.
CKE[3:0]	O CMOS	**SDRAM Clock Enable:** CKE[3:0] are used for signaling powerdown entry, powerdown exit, self refresh entry, and self refresh exit commands to an SDRAM row. There is one CKE signal per row (CKE0 for row 0, CKE1 for Row 1, CKE2 for Row 2 and CKE3 for Row 3).
SCLKA SCLKB	O CMOS	**SDRAM Clocks:** SCLKA and SCLKB are two copies of the SDRAM clock generated by the MTH. External buffers may be required to generate an adequate number of clocks required by the DIMM. Each clock must have 4-5 loads.
SCLKFDBK	I CMOS	**SDRAM Clock Feed Back:** SCLKFDBK is the SDRAM clock feed back for DLL use.

2.3. Power, Reference, Reset, and Test Signals

Table 6. Reset and Test Signals (3.3V)

Signal	Type	Description
TESTIN#	I CMOS	**Test Input:** TESTIN# is used for manufacturing and board level test purposes. This signal is sampled on the rising edge of RST#. This signal must be pulled up externally through an 8.2 KΩ resistor to 3.3V.
RST#	I CMOS	**Reset:** When asserted, RST# asynchronously resets the MTH logic. RST# must **not** be asserted during STR.

Table 7. Power, Ground, and Reference Signals

Signal	Description
RAMREF[A:B]	**Rambus* Reference:** Reference voltage input for the Rambus* RSL interface.
VCC3_3	**3.3 Volt Power:** Power pins for SDRAM interface, RST# & TESTIN#.
VCC2_5	**2.5 Volt Power:** Power pins for MTH core.
VCC1_8	**1.8 Volt Power:** Power pins for Rambus* interface.
VSS	**Ground:**

3. Register Description

The MTH has internal configuration and control registers. These registers are accessed through the Rambus* CMOS signal interface. In the MTH, each register is addressed as an entity; therefore, each register needs only one address.

Register Terminology and Definitions

Symbol	Description
RO	Read Only. If a register is read only, writes to this register have no effect.
R/W	Read/Write. A register with this attribute can be read and written
Reserved Bits	Some of the MTH registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back.
Default Value	Upon a Full Reset, the MTH sets all of its internal configuration registers to predetermined **default** states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the MTH registers accordingly.

3.1. MTH Registers

3.1.1. MDID—MTH Device ID Register

Address: 02h
Default: 0009h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:6	Reserved
5:4	**Device ID Mode Select:** 00 = The Device ID [3:0] in the MCP packet is compared against the MTH Device ID[3:0] to identify the selected MTH. In this mode, only one SDRAM row of the MTH can be used. The selected SDRAM row is always zero. 01 = The Device ID [3:1] in the MCP packet is compared against the MTH Device ID[3:1] to identify the selected MTH. The Device ID[0] of the MCP packet is used to identify the selected SDRAM row. In this mode, only two SDRAM rows of the MTH can be used. 10 = Reserved. 11 = The Device ID [3:2] in the MCP packet is compared against the MTH Device ID[3:2] to identify the selected MTH. The Device ID[1:0] of the MCP packet is used to identify the selected SDRAM row. In this mode, all four SDRAM rows of the MTH can be used.
3:0	**MTH Device ID:** This field specifies the device ID of the MTH. This field is compared against the Device ID field of the MCP packet to determine if this is the addressed MTH device.

3.1.2. MTR—MTH Timing Register

Address: 03h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15	**Second Copy of Control Signals (DCS) Disable:** 1 = Disable. MTH disables (drives low) the control signals intended for rows 2 and 3. The disabled control signals are: MAB[12:0], BAB[1:0], RASB#, CASB#, WEB#, CSA/B[3:2] CKE[3:2]. 0 = Enable.
14	**SCLKB Disable:** 1 = Disable. The SCLKB output pin is disabled. 0 = Enable.
13	**ECC Mode Enable:** 1 = Enable. The MTH passes the ECC code it received through the data packet to the SDRAM interface. It does not check the ECC code for errors. 0 = Disable. The MTH does not support ECC. In ECC mode byte masking is not supported.
12	**MTH Disable:** 1 = Disable. The MTH is functionally disabled. The MTH does not monitor the input signals or drives the output signals. When MTH is disabled, its serial interface signals (SIO0, SIO1, CMD and SCK) do function as normal. (Default). A reset (RST# active) has to be applied to the MTH to get it out of the disabled mode. 0 = Enable.
11:10	Reserved.
9	**Registered DIMM Timing Enable (RDTE):** 1 = Enable. Registered DIMM timings are assumed for SDRAM operation. Thus, the CL = 2 is interpreted as CL =3 and CL = 3 is interpreted as CL =4. Also, the write data has to be sent one cycle later than normal to the SDRAM. Registered DIMMs must be CL=2. CL=3 will not function for Registered DIMMs. 0 = Disable
8	**Relaxed SDRAM Timing Enable (RSTE):** 1 = Enable. Two cycle rule (2n) for accessing the SDRAM must be employed. The two cycle rule defines that the MA and the other control signals (RAS, CAS, WE, and DQM) for SDRAM must be set up one cycle before CS# is applied. 0 = Disable. The CS# is asserted at earliest possible cycle. MA and other control signals may be flowing through to SDRAM before CS# is asserted.
7:6	Reserved.

Bit	Descriptions
5:4	**Read Command to Read Data Delay (tCAC):** This field defines the minimum delay from read command to read data on the Direct Rambus* channel. The tCAC value is dependent on the value of the RSTE bit. The tCAC values below are in RDRAM channel clocks. **Bit[5:4] RSTE = 0 RSTE = 1** 00 15 18 01 19 22 10 23 26 11 27 30 All other combinations reserved
3	**CAS Latency (tCL):** This bit specifies the number of SCLKs between when a read command is sampled by the SDRAMs and when the MTH samples read data from the SDRAMs. 0 = 2 1 = 3
2:0	**Direct Rambus* Channel Levelization Delay:** This field specifies the amount of levelization required in the MTH to levelize the read data going onto the expansion channel. The delay shown below is in RCLKs. 000 = 0 100 = 4 001 = 1 101 = 5 010 = 2 110 = 6 011 = 3 111 = 7 All other combinations reserved

3.1.3. MOR—MTH Operation Register

Address: 04h
Default: 0000h
Access: Bits 7:6 Read/Write, Bits 5:0 Read only
Size: 16 bits

Bit	Descriptions
15:7	Reserved.
8	**SDRAM Initalization Done (SID)—R/W:** BIOS must set this bit to indicate the completion of SDRAM initialization. The inverted version of this bit drives the DQM pin. This bit has to be set to 1 by BIOS before it attempts to read or write the SDRAM memory.
7	**Broadcast SDRAM Initialization Command (Broadcast SIC) —R/W:** 1 = SIC command specified by bits [2:0] is issued to all four SDRAM rows. 0 = SIC command specified by bits [2:0] is issued to only the row specified by Row Select field (bits [4:3]).
6	**Mode Register Set (MRS) Field—R/W:** This bit defines the value of A[12:0] to be used with MRS command. Note that these values are the values seen by SDRAMs on their A[12:0] pins. 0 = 0031h (values seen by SDRAMs on their A[12:0] pins) 1 = 0021h (values seen by SDRAMs on their A[12:0] pins)
5	**Initiate SIC Operation—RO:** 1 = Execute SIC command specified by bits[2:0]. 0 = MTH sets to 0 after execution completes. Software must check to see if this bit is zero before writing to this bit.
4:3	**Row Select(RS) —RO:** Specifies the SDRAM row to be used with SIC field. 00 = Row 0 01 = Row 1 10 = Row 2 11 = Row 3
2:0	**SDRAM Initialization Command (SIC) —RO:** This field allows the MTH to issue various commands to the SDRAM row specified by bits[4:3]. BIOS uses this field to initialize the SDRAMs. The BIOS programs this field with appropriate command and sets bit 5 to a 1. When the MTH sees bit 5 set to 1, it executes the command specified by the SIC field. At the end of the command execution, the MTH sets bit 5 to 1. 001 = **NOP Command:** When the MTH receives this command, it issues a NOP command to the SDRAM row specified by bits[4:3]. 010 = **All Banks Precharge:** When the MTH receives this command, it issues an All Banks Precharge command to the SDRAM row specified by bits[4:3]. 011 = **Mode Register Set:** When the MTH receives this command, it issues a Mode Register Set (MRS) command to the SDRAM row specified by bits [4:3]. Bit 6 of this register defines the value of A[12:0] to be used with this command. 100 = **Burst CAS before RAS (CBR):** When the MTH receives this command, it issues eight CBR commands to the SDRAM row specified by bits [4:3]. CBR is an Auto Refresh command. 101 = **Assert CKE:** When MTH receives Command it assert All other combinations reserved.

3.1.4. MBSCRA—Memory Buffer Strength Control Register A

Address: 05h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:14	**MD[63:0] Buffer Strength:** This field sets the buffer strengths for the MD[63:0] pins. 00 = 1x 01 = Reserved 10 = 2x 11 = Reserved
13:12	**MECC[7:0]/DQM[7:0] Buffer Strength:** This field sets the buffer strengths for the MECC[7:0]/DQM[7:0] pins. 00 = 1x 01 = Reserved 10 = 2x 11 = Reserved
11	**CS0[B:A]# Buffer Strength:** This field sets the buffer strengths for the CS0[B:A]# pins. 0 = 1x 1 = 2x
10	**CS1[B:A]# Buffer Strength:** This field sets the buffer strengths for the CS1[B:A]# pins. 0 = 1x 1 = 2x
9	**CS2[B:A]# Buffer Strength:** This field sets the buffer strengths for the CS2[B:A]# pins. 0 = 1x 1 = 2x
8	**CS3[B:A]# Buffer Strength:** This field sets the buffer strengths for the CS3[B:A]# pins. 0 = 1x 1 = 2x
7:6	**CKE3 Buffer Strength:** This field sets the buffer strength for the CKE3 pin. 00 = 1x 01 = reserved 10 = 2x 11 = 3x
5:4	**CKE2 Buffer Strength:** This field sets the buffer strength for the CKE2 pin. 00 = 1x 01 = Reserved 10 = 2x 10 = 3x
3:2	**CKE1 Buffer Strength:** This field sets the buffer strength for the CKE1 pin. 00 = 1x 01= Reserved 10 = 2x 11= 3x
1:0	**CKE0 Buffer Strength:** This field sets the buffer strength for the CKE0 pin. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x

3.1.5. MBSCRB—Memory Buffer Strength Control Register B

Address: 06h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:8	Reserved
7:6	**MAA[12:0], BAA[1:0], RASA#, CASA#, WEA# Buffer Strength:** This field sets the buffer strengths for MAA[12:0], BAA[1:0], RASA#, CASA#, and WEA# pins. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x
5:4	**MAB[12:0], BAB[1:0], RASB#, CASB#, WEB# Buffer Strength:** This field sets the buffer strengths for MAB[12:0], BAB[1:0], RASB#, CASB#, and WEB# pins. 00 = 1x 01 = Reserved 10 = 2x 11 = 3x
3:0	Reserved.

3.1.6. EXCC—Direct Rambus* Current Register

Address: 07h
Default: 0000h
Access: Read/Write
Size: 16 bits

Bit	Description
15:7	Reserved
6:0	**Current Control:** This 7-bit field controls the current for the DQA[8:0] and DQB[8:0] RSL pins. For details, refer to the *Direct Rambus** Technical Specification*.

3.1.7. RIR—RAC Initialization Register

Address: 09h
Default: 0000h
Access: Read/Write, Read Only
Size: 16 bits

Bit	Description
15:6	Reserved
5	**Ready for Synchronization Packet—RO:** BIOS must check this bit before sending the Synchronization packet to the MTH. 1 = Ready. The MTH sets this bit when it is ready to accept the Synchronization MCP packet. 0 = Not Ready.
4	**RAC Initialization Complete (RC)—RO:** BIOS must check this bit to make sure the RAC is properly initialized before initiating memory accesses. 1 = Complete.The MTH sets this bit after it has completed RAC initialization. 0 = Not Complete
3	**Initiate RIC Operation (IRO)—R/W:** BIOS must check to see if this bit is 0 before writing to this bit. 1 = Executing. Execution of the RIC command specified by bits[2:0] starts. 0 = Not Executing. After execution completes, the MTH clears this bit to 0.
2:0	**RAC Initialization Command (RIC)—R/W:** This field allows BIOS to initialize MTH RAC. BIOS programs this field with the appropriate command and sets IRO (bit[3]) to 1. When the MTH sees bit[3] set to 1, it executes the command specified by the RIC field. At the end of command execution, the MTH sets bit 3 to 0. 000 = Reserved 001 = **Initialize RAC:** When the MTH receives this command, it performs an initialization sequence on the MTH RAC. The initialization process includes executing the power-up sequence to the MTH RAC and Current and Temperature Calibrating of the MTH RAC. 010 = **Manual Current Calibrate the RAC:** When the MTH receives this command, it issues a manual Current Calibrate sequence to the RAC. The Current Control value specified in the EXCCA register is used as the manual current control value. 011 = **Temperature Calibrate the RAC:** When the MTH receives this command, it issues a Temperature Calibrate sequence to the RAC. 100 = **Set Fast Clock Mode:** When the MTH receives this command, it issues a Set Fast Clock Mode sequence to the RAC. All other combinations reserved.

3.1.8. INIT—MTH Initialization Register

Address: 21h
Default: 0009Fh
Access: Read/Write
Size: 16 bits

Bit	Descriptions
15:8	Reserved.
7	**SIO repeater bit (SRP):** This bit controls the value on SIO1 pin. SIO1 = SIO0 when SRP = 1. SIO1 = 1 when SRP = 0. After an SIO Reset command is executed, SRP is 1.
6:5	Reserved.
4:0	**Serial ID:** This field specifies Serial ID of the MTH. The serial ID is compared against the serial address in initialization request packets to determine if this is the addressed MTH device. The default value of Serial ID is 1Fh

3.1.9. RACB—RAC Configuration Register B

Address: 0Bh
Default: 0000h
Access: Read/ Write
Size: 16 bits

Overall performance of the RSL channel is specific to individual motherboard design. If a design exhibits marginalities in the RSL channel, performance can be further optimized by enabling E-clamps or On-die termination, or both.

Enabled by the register settings shown below, E-clamps and On-die termination provide an MTH-internal voltage clamping mechanism to reduce overshoot and undershoot on the RSL channel; This effectively minimizes layout related mis-matching between the device package and the motherboard.

If channel overshoot and undershoot are found, E-clamps should be enabled first, followed by On-die termination if E-clamps alone do not improve channel matching.

Note: On-die termination should not be confused with RSL channel termination that is required whether On-die termination is enabled or not.

To enable MTH E-clamps or On-die Termination, the following bits should be set:

- 0300h to enable E-clamps (RAC Configuration bits [25,24])
- 0400h to enable On-die Termination (RAC Configuration bits [26])
- 0700h to enable both (RAC Configuration bits [26:24])

Bit	Description
15:11	Reserved
10	**On-Die Termination Enable:** 1 = Enable On –Die Termination 0 = Disable
9:8	**E-Clamps Enable:** Set bits 9:8 to enable E-Clamps 11 = Enable 01 = Reserved 10 = Reserved 00 = Disable
7:0	Reserved

3.1.10. VID—Vendor Identification Register

Address: 35h
Default: 8086h
Access: Read only
Size: 16 bits

Bit	Descriptions
15:0	**Vendor Identification Number (VID):** This is a 16 bit value assigned to Intel. Intel VID = 8086h.

3.1.11. RID—Revision Identification Register

Address: 36h
Default: 0000h
Access: Read only
Size: 16 bits

Bit	Descriptions
15:8	Reserved
7:0	**Revision Identification Number:** This is an 8 bit field that identifies the revision identification number for MTH. A0 = 00h A1 = 01h B0 = 02h B1 = 03h

3.1.12. DID—Device Identification Register

Address: 37h
Default: 2520
Access: Read only
Size: 16 bits

Bit	Descriptions
15:0	**Device Identification Number:** This is a 16 bit value assigned to MTH. MTH = 2520h

4. Functional Description

4.1. Operational Overview

When the MTH receives a command from the MCH, it decodes the command and drives the appropriate signals on the SDRAM interface. For read commands, the MTH receives data from the SDRAMs and then converts the data to the appropriate Direct Rambus* packet format before sending it to the MCH. The MTH is aware of the CAS Latency (CL) for the SDRAMs and adjusts the timings accordingly.

The MTH supports a modified version of RDRAM write protocol on the Direct Rambus* channel. To provide this support, the MTH contains a write buffer to temporarily store the write data and control from the MCH. It stores this data to SDRAM after receiving a Retire command (implied or explicit) from the MCH.

The MTH also supports the Current Calibration and Temperature Calibration of the Direct Rambus* channel after receiving the commands from MCH.

The MTH contains registers for configuration and control. These registers are accessed through the CMOS interface provided by the Direct Rambus* channel.

4.2. Protocol Overview

For the Direct Rambus* Channel, there are two groups of high speed RSL signals (high speed RSL data and control bus).

There is also a group of low speed CMOS control signals. The control signal groups are referred to as the Request Control (RQ); the data signals are referred to as DQA and DQB signals. The Request Control signals carry the Memory Control Packets (MCP) from the MCH to the MTH.

4.2.1. Packet Format

A command packet uses all 8 RSL request signals (RQ[7:0]) on the channel to send the command from the MCH to the MTH. This command packet is known as MCP (Memory Control Packet). There are 32 bits in a MCP packet. The MCP packet is sent over the channel in two RDRAM clocks (RClks).

4.2.2. SDRAM Command Truth Table

The following table shows the SDRAM command encoding for the respective MCP commands.

Table 8. SDRAM Command Encoding For Respective MCP Commands

Function	SCLK n	SCLK n-1	CKE n	CKE n-1	CS#	RAS#	CAS#	WE#	A11	A10	BA[1:0]	A9-A0
NOP	R	R	H	x	L	H	H	H	x	x	x	x
Read	R	R	H	x	L	H	L	H	V	L	V	V
Read with autoprecharge	R	R	H	x	L	H	H	V	V	H	V	V
Write	R	R	H	x	L	H	L	L	V	L	V	V
Write with autoprecharge	R	R	H	x	L	H	L	L	V	H	V	V
Bank Activate	R	R	H	x	L	L	H	H	V	V	V	V
Precharge selected bank	R	R	H	x	L	L	H	L	V	L	x	x
Precharge all banks	R	R	H	x	L	L	H	L	x	H	x	x
Refresh	R	R	H	H	L	L	L	H	x	x	x	x
Self Refresh Entry	R	R	H	L	L	L	L	H	x	x	x	x
Self Refresh Exit	R	R	L	H	H	x	x	x	x	x	x	x
Powerdown Entry	R	R	H	L	H	x	x	x	x	x	x	x
Powerdown Exit	R	R	L	H	H	x	x	x	x	x	x	x
Mode Register Set	R	R	H	x	L	L	L	L	L	L	V	V
Clock Stop	R	L	x	x	x	x	x	x	x	x	x	x

NOTES:

1. x = Don't care, H = Logic high, L = Logic Low, R = Clock running, V = Valid address

4.2.3. Current Calibration

After receiving the Current Calibrate and Current Calibrate and Sample commands from MCH, the MTH initiates the current calibrate process of its Direct Rambus* interface.

4.2.4. Temperature Calibration

After receiving the Temperature Calibrate command from MCH, the MTH initiates temperature calibration process of its RAC.

4.2.5. SDRAM CAS-before-RAS (CBR) Refresh

The MTH supports only CBR for active refresh. It sends the CBR command to an SDRAM row when it receives the appropriate MCP from MCH. Also, the MTH sends eight consecutive CBR commands (appropriately timed) to the specified SDRAM row After receiving a Burst CBR serial command through the MOR register.

4.2.6. Self Refresh Entry and Exit

The MTH supports self refresh entry and exit commands.

4.2.7. Powerdown Entry and Exit

The MTH supports Powerdown Entry and Exit commands to SDRAMs.

4.2.8. SDRAM Command Issue Rules

The MTH supports two timing modes for sending commands to SDRAM. These modes are known as “1 Cycle” and “2 Cycle” command timing rules.

“1 Cycle” Command Rule

In this mode the MA, RAS#, CAS#, and WE# control signals are driven to an SDRAM row in the same clock (SCLK) that CS# is driven for that row.

“2 Cycle” Command Rule

In this mode the MA, RAS#, CAS#, and WE# control signals are driven to an SDRAM row one clock (SCLK) earlier than the CS# is driven for that row.

4.2.9. Write Operation Policy

The MTH implements a modified version of the RDRAM write protocol as described below. The MTH implements a write buffer that temporarily store the write data, address, and control for up to two write commands from MCH. A 16-byte data packet from the write buffer is sent to SDRAM when a Retire command (explicit or implicit) is received by the MTH. If the Retire command specifies masked retire, then the mask bits in the Retire command must be used as DQM signals for writes to the SDRAM.

The rules for write operations are:

- The write data must be sent 1 or 2 Direct Rambus* channel clocks (depending on Host bus frequency) after the write MCP packet is sent.
- A MCP to retire the data that is in the MTH to SDRAM must be sent along with the data packet. One of the following MCPs will retire data to the SDRAM.
  - A Retire MCP to the same MTH
  - A Write MCP to a different MTH or a Read MCP to a different MTH must be sent along with the data packet. This retires the data to SDRAM.

4.2.10. ECC Support

The MTH supports the ECC feature by passing the ECC code from the Direct Rambus* channel to SDRAM and vice versa. The MTH does not monitor the data for errors as it passes between the Direct Rambus* channel and the SDRAM array. If ECC is enabled, byte masking is disabled.

4.2.11. SDRAM Initialization

BIOS initializes the SDRAM by programming the MOR register in the MTH. This register is accessed through the Direct Rambus* CMOS interface signals SCK, SIO and CMD.

4.2.12. Suspend to RAM Support

The MTH supports the STR power management state by maintaining the appropriate states on the SDRAM interface signals. The system puts the MTH in the STR state by executing the following sequences:

- Issue Self Refresh entry commands to all SDRAM rows
- Issue Stop Clock command to MTHs. After receiving this command, the MTH power downs the MTH RAC and then turns off the SDRAM PLL. This turns off the SCLKs going to SDRAM rows.
- Turn off the system clock generators.

The VCC power to the MTH must be maintained during STR. The following power sources must be kept alive to the MTH during STR:

- VCC2_5 (MTH core)
- VCC1_8 (SCK, CMD, and SIO interface)
- VCC3_3 (SDRAM interface)

Note: MTH RST should **NOT** be toggled entering or exiting STR (ACPI S3).

During STR exit, BIOS initializes the MTH RAC, after the Rambus* channel clock is stable. The initialization includes current and temperature calibration of the RAC. BIOS then issues a synchronization packet to the MTH. This starts the SDRAM clocks (SCLKs). The Self Refresh Exit can be issued after the MTHs are levelized.

4.2.13. System Clocking

The MTH receives the differential Direct Rambus* clock from the DRCG clock generator chip in the system. From this clock the MTH generates two copies of SCLK for SDRAM use. A feedback input (SCLKFDBK) is provided on the MTH to connect to an output from the clock buffer for phase alignment.

4.2.14. SDRAM Timing Parameters

The MTH only needs one SDRAM timing parameter to operate properly. This timing parameter is CAS Latency (CL). All other SDRAM timing parameters are taken care of by MCH.

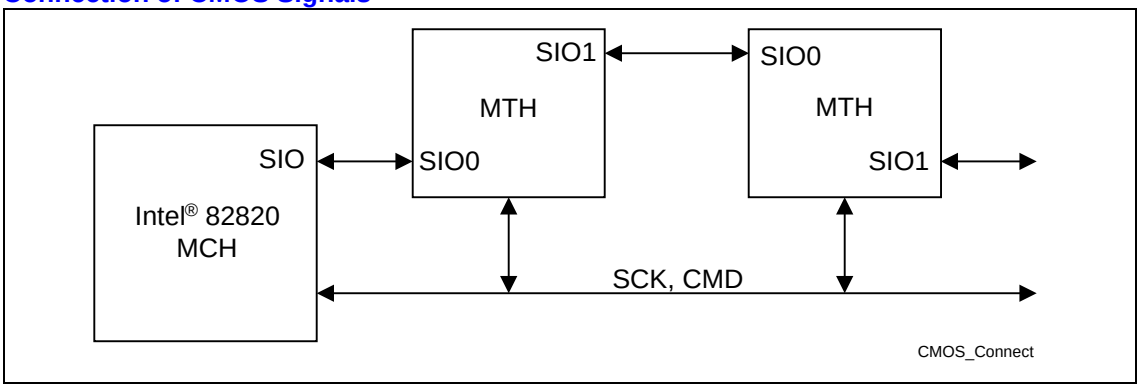
4.3. CMOS Protocol

4.3.1. Overview

The CMOS interface signals and protocol on the Direct Rambus* Channel are used for MTH initialization and MTH register accesses.

The connection of Direct Rambus* CMOS signals between MCH and MTH is illustrated in **Figure 3** .

Figure 3: Connection of CMOS Signals



Using the Rambus* CMOS interface, control packets are passed from MCH to MTH. The control packet may be directed to individual MTHs or broadcast to all MTHs.

4.3.2. Serial Control Packet Formats

Four types of Direct Rambus* serial control packets are defined for use on the Direct Rambus* channel:

- Serial Request Packets (SRQ)
- Serial address (SA)
- Serial Interval (SINT)
- Serial Data (SD)

Figure 4, **Figure 5** and **Figure 6** show the layout of Register Read, Register Write and Non-Register Operation packet types.

Figure 4: Direct Rambus* Serial Control Packet Format for Register Read

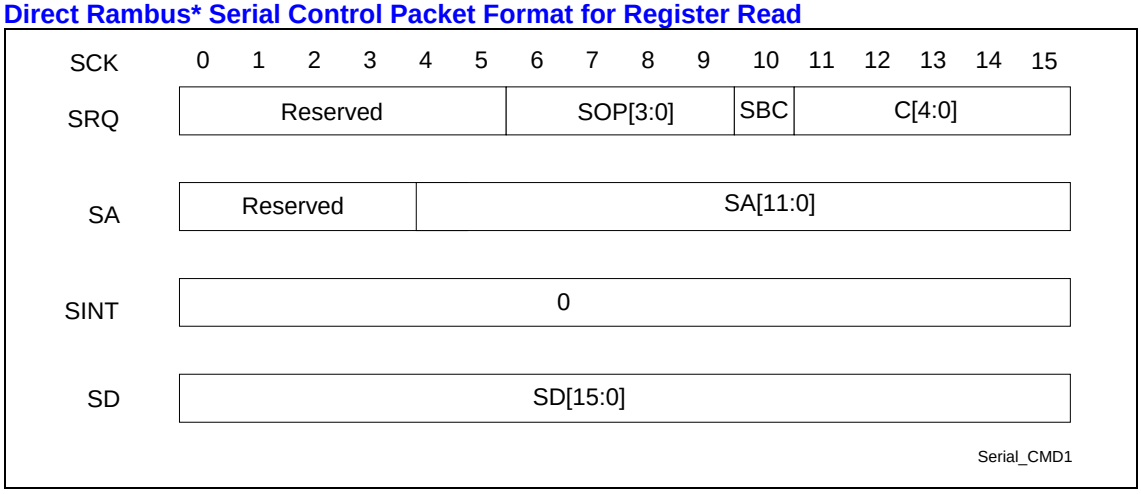


Figure 5: Direct Rambus* Serial Control Packet Format for Register Write

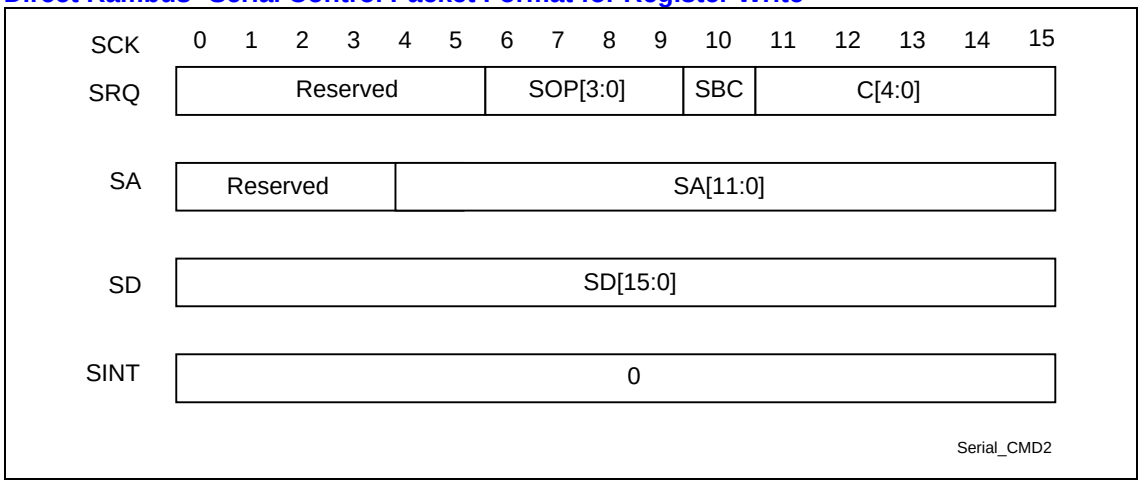
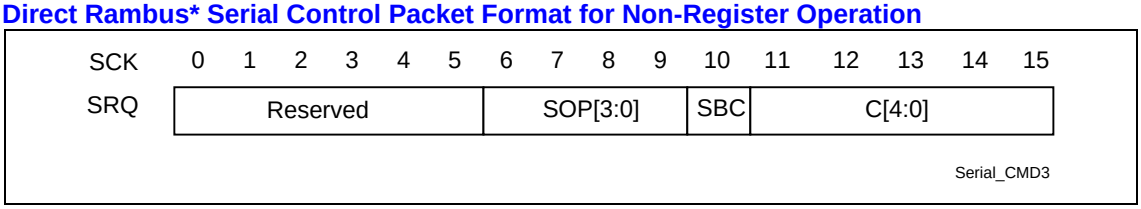


Figure 6. Direct Rambus* Serial Control Packet Format for Non-Register Operation



Note that these packet formats are the same as those used by the Direct RDRAM devices. Table 9 describes each of the fields for these serial packets.

Table 9. Direct Rambus* Serial Packet Field Definitions

Field	Description
SOP[3:0]	**Serial Op-code (SOP):** This field specifies the command for control register operations. Encodings not listed are reserved. 0000 - SRD: Serial read of the register specified in SA[11:0] from MTH specified by C[4:0]. 0001 - SWR: Serial write of the register specified in SA[11:0] from MTH specified by C[4:0].
SBC	**Serial Broadcast:** 1 = All MTHs execute the specified SOP command.
C[4:0]	**MTH Serial Address:** C[4:0] are compared to bits [3:0] of the MDID register to select the MTH that the Direct Rambus* serial transaction is directed.
SA[11:0]	**Serial Register Address:** SA [11:0] selects which control register of the selected MTH is read or written.
SD[15:0]	**Serial Data:** The 16 bits of data read from or written to the selected control register in the selected MTH.

The following sections detail the available packet formats and the operations that can be performed on the serial control bus.

4.3.3. Transactions

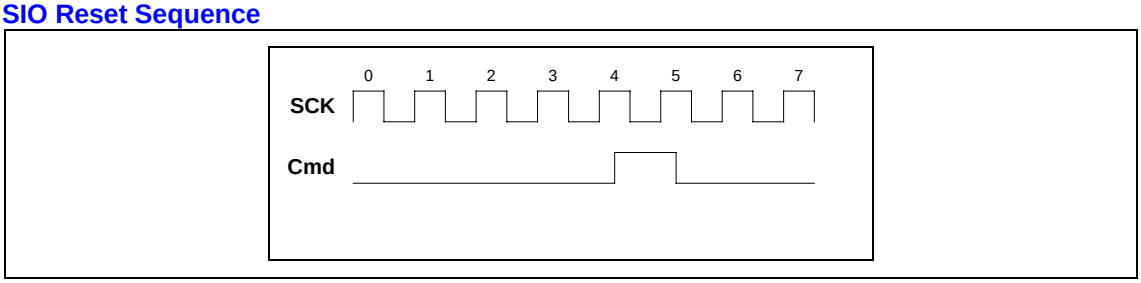
Reset

After power-on, the MTHs in the memory system must be reset. This process is:

1. Reset the SIO chain that connects the MTHs together.
2. Reset all MTHs on the Direct Rambus* channel using serial control packets. At this point a register read can be issued to determine if the devices connected on the Direct Rambus* channel are MTHs or other types of Direct Rambus* devices.

First, the SIO serial chain (SIO0-SIO1-SIO0) is reset by issuing an SIO reset sequence as shown Figure 7.CMD is sampled on both the rising and falling edges of SCK. An 1100 sequence on CMD resets the state machine controlling the SIO pins in each MTH. After this reset, the SIO pin is configured as an input and SIO1 pin is configured as an output on every MTH. Also the SIO repeater bit in MTH is set to 1.

Figure 7. SIO Reset Sequence



Initialization

The following steps are performed to initialize the memory subsystem after reset.

1. Assign unique serial addresses to all MTHs.
2. Read all read-only registers and process the information.
3. Update the necessary read-write registers.
4. Assign unique device ID's to each RDRAM and channel ID's to each MTH.
5. Repeat steps 1 to 3 for all MTHs.
6. Levelize the Direct Rambus* Channel.

MTH Register Operations

Figure 8 shows the control register read operation and Figure 9 shows the control register write operation.

Figure 8. MTH Register Read

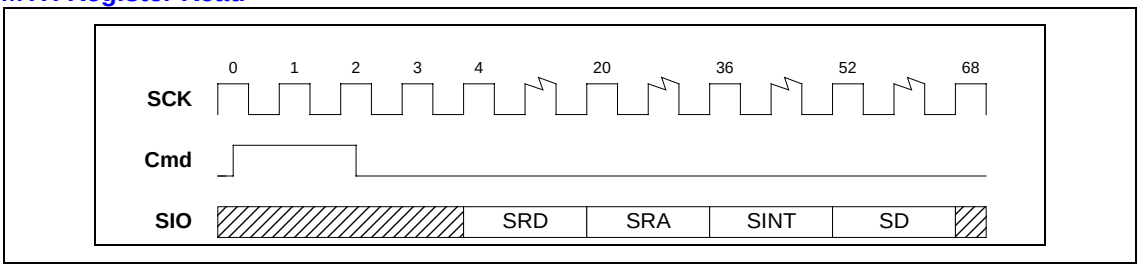
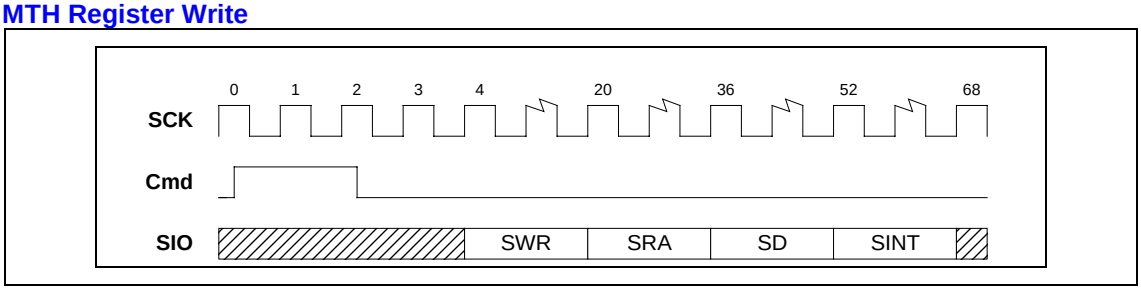


Figure 9. MTH Register Write



5. Ballout and Package Specifications

5.1. Ballout Information

Figure 10. MTH Ballout (Top View—Left Side)

	1	2	3	4	5	6	7	8	9
A	VSS	VSS	DQA8	DQA6	DQA2	DQA0	CFM	CTM#	RQ6
B	VSS	VCC2_5	VSS	VSS	DQA4	VSS	CFM#	CTM	VSS
C	VSS	VCC2_5	DQA7	DQA5	DQA3	DQA1	VSS	VSS	RQ7
D	DQMIN	VSS	VSS	VSS	VSS	VCC2_5	VSS	REFA	REFB
E	MD62	TESTIN#	MD63	VCC2_5	VCC2_5	VCC2_5	VCC2_5		VCC2_5
F	MD61	VSS	MD31	RST#	VCC3_3				
G	MD59	MD60	MD29	MD30	VCC3_3				
H	MD57	MD58	MD26	MD28				VSS	VSS
J	MD56	MD24	VSS	MD27	VCC3_3			VSS	VSS
K	MD55	MD23	MD22	MD25				VSS	VSS
L	MD53	MD21	MD54	MD20	VCC3_3				
M	MD51	MD52	VSS	MD19	VCC3_3				
N	MD18	CKE1	CKE3	MD17	VCC2_5	VCC3_3	VCC3_3		VCC3_3
P	MD16	MD49	MD50	CSA1#	CSB1#	MAA11	MAB11	MAA7	MAB7
R	SCLKB	VCC3_3	MD48	CSA2#	BAB0	BAA0	VSS	MAA8	MAB8
T	SCLKA	DQM7/ MECC7	DQM2/ MECC2	CSB2#	CKE0	BAB1	MAB12	MAA9	MAB9
U	VSS	SCLKFDBK	DQM6/ MECC6	DQM3/ MECC3	CKE2	BAA1	MAA12	MAA10	MAB10
	1	2	3	4	5	6	7	8	9

Note: The MECC balls are also the respective DQM balls.

Figure 11: MTH Ballout (Top View—Right Side)

10	11	12	13	14	15	16	17	
RQ5	RQ2	RQ0	DQB3	DQB5	DQB7	SCK	CMD	A
RQ4	VSS	DQB1	VSS	DQB6	VSS	VSS	VCC1_8	B
RQ3	RQ1	DQB0	DQB2	DQB4	DQB8	SIO0	SIO1	C
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	D
	VCC2_5	VCC2_5	VCC2_5	MD0	MD1	MD33	MD32	E
			VCC3_3	MD2	MD3	MD35	MD34	F
			VCC3_3	MD4	MD5	VSS	MD36	G
VSS				MD6	MD7	MD38	MD37	H
VSS			VCC3_3	MD8	VSS	MD40	MD39	J
VSS				VSS	MD10	MD9	MD41	K
			VCC3_3	MD12	MD11	MD43	MD42	L
			VCC3_3	MD13	VSS	MD45	MD44	M
	VCC3_3	VCC3_3	VCC2_5	MD15	MD47	MD14	MD46	N
MAA6	MAB6	MAA0	MAB0	WEA#	CASA#	WEB#	CASB#	P
VSS	MAB5	MAA1	MAB1	DQM4/ MECC4	DQM0/ MECC0	VSS	DQM1/ MECC1	R
MAA5	MAA2	MAB2	VSS	DQM5/ MECC5	CSB3#	CSA3#	CSA0#	T
MAA4	MAB4	MAA3	MAB3	CSB0#	RASB#	RASA#	VSS	U
10	11	12	13	14	15	16	17	

Note: The MECC balls are also the respective DQM balls.

Table 10. MTH Alphabetical Ballout List

Signal	Ball #
BAA0	R6
BAA1	U6
BAB0	R5
BAB1	T6
CASA#	P15
CASB#	P17
CFM	A7
CFM#	B7
CKE0	T5
CKE1	N2
CKE2	U5
CKE3	N3
CMD	A17
CSA0#	T17
CSA1#	P4
CSA2#	R4
CSA3#	T16
CSB0#	U14
CSB1#	P5
CSB2#	T4
CSB3#	T15
CTM	B8
CTM#	A8
DQA0	A6
DQA1	C6
DQA2	A5
DQA3	C5
DQA4	B5
DQA5	C4
DQA6	A4
DQA7	C3
DQA8	A3
DQB0	C12
DQB1	B12
DQB2	C13

Signal	Ball #
DQB3	A13
DQB4	C14
DQB5	A14
DQB6	B14
DQB7	A15
DQB8	C15
DQM0/ MECC0	R15
DQM1/ MECC1	R17
DQM2/ MECC2	T3
DQM3/ MECC3	U4
DQM4/ MECC4	R14
DQM5/ MECC5	T14
DQM6/ MECC6	U3
DQM7/ MECC7	T2
DQMIN	D1
MAA0	P12
MAA1	R12
MAA2	T11
MAA3	U12
MAA4	U10
MAA5	T10
MAA6	P10
MAA7	P8
MAA8	R8
MAA9	T8
MAA10	U8
MAA11	P6
MAA12	U7
MAB0	P13
MAB1	R13

Signal	Ball #
MAB2	T12
MAB3	U13
MAB4	U11
MAB5	R11
MAB6	P11
MAB7	P9
MAB8	R9
MAB9	T9
MAB10	U9
MAB11	P7
MAB12	T7
MD0	E14
MD1	E15
MD2	F14
MD3	F15
MD4	G14
MD5	G15
MD6	H14
MD7	H15
MD8	J14
MD9	K16
MD10	K15
MD11	L15
MD12	L14
MD13	M14
MD14	N16
MD15	N14
MD16	P1
MD17	N4
MD18	N1
MD19	M4
MD20	L4
MD21	L2
MD22	K3
MD23	K2

Signal	Ball #
MD24	J2
MD25	K4
MD26	H3
MD27	J4
MD28	H4
MD29	G3
MD30	G4
MD31	F3
MD32	E17
MD33	E16
MD34	F17
MD35	F16
MD36	G17
MD37	H17
MD38	H16
MD39	J17
MD40	J16
MD41	K17
MD42	L17
MD43	L16
MD44	M17
MD45	M16
MD46	N17
MD47	N15
MD48	R3
MD49	P2
MD50	P3
MD51	M1
MD52	M2
MD53	L1
MD54	L3
MD55	K1
MD56	J1
MD57	H1
MD58	H2

Signal	Ball #
MD59	G1
MD60	G2
MD61	F1
MD62	E1
MD63	E3
RASA#	U16
RASB#	U15
REFA	D8
REFB	D9
RQ0	A12
RQ1	C11
RQ2	A11
RQ3	C10
RQ4	B10
RQ5	A10
RQ6	A9
RQ7	C9
RST#	F4
SCK	A16
SCLKA	T1
SCLKB	R1
SCLKFDBK	U2
SIO0	C16
SIO1	C17
TESTIN#	E2
VCC1_8	B17
VCC2_5	B2

Signal	Ball #
VCC2_5	C2
VCC2_5	D6
VCC2_5	E4
VCC2_5	E5
VCC2_5	E6
VCC2_5	E7
VCC2_5	E9
VCC2_5	E11
VCC2_5	E12
VCC2_5	E13
VCC2_5	N5
VCC2_5	N13
VCC3_3	F5
VCC3_3	F13
VCC3_3	G5
VCC3_3	G13
VCC3_3	J5
VCC3_3	J13
VCC3_3	L5
VCC3_3	L13
VCC3_3	M5
VCC3_3	M13
VCC3_3	N6
VCC3_3	N7
VCC3_3	N9
VCC3_3	N11
VCC3_3	N12

Signal	Ball #
VCC3_3	R2
VSS	A1
VSS	A2
VSS	B1
VSS	B3
VSS	B4
VSS	B6
VSS	B9
VSS	B11
VSS	B13
VSS	B15
VSS	B16
VSS	C1
VSS	C7
VSS	C8
VSS	D2
VSS	D3
VSS	D4
VSS	D5
VSS	D7
VSS	D10
VSS	D11
VSS	D12
VSS	D13
VSS	D14
VSS	D15
VSS	D16

Signal	Ball #
VSS	D17
VSS	F2
VSS	G16
VSS	H8
VSS	H9
VSS	H10
VSS	J3
VSS	J8
VSS	J9
VSS	J10
VSS	J15
VSS	K8
VSS	K9
VSS	K10
VSS	K14
VSS	M3
VSS	M15
VSS	R7
VSS	R10
VSS	R16
VSS	T13
VSS	U1
VSS	U17
WEA#	P14
WEB#	P16

5.2. Package Information

This section shows the mechanical dimensions for the MTH. The package is a 241 Ball Grid Array (BGA).

Figure 12. Package Dimensions (241 BGA) – Top and Side Views

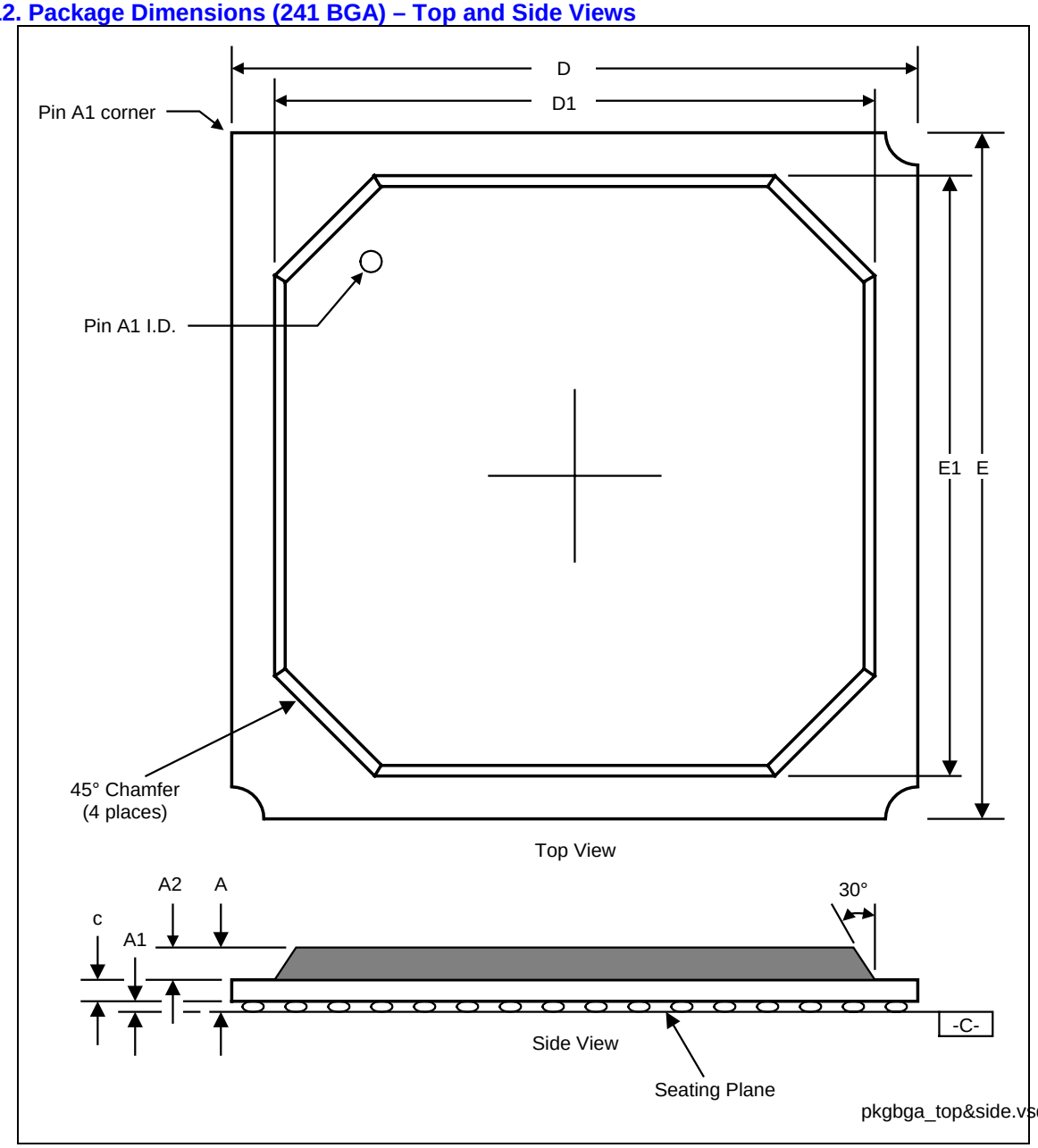


Figure 13. Package Dimensions (241 BGA) – Bottom View

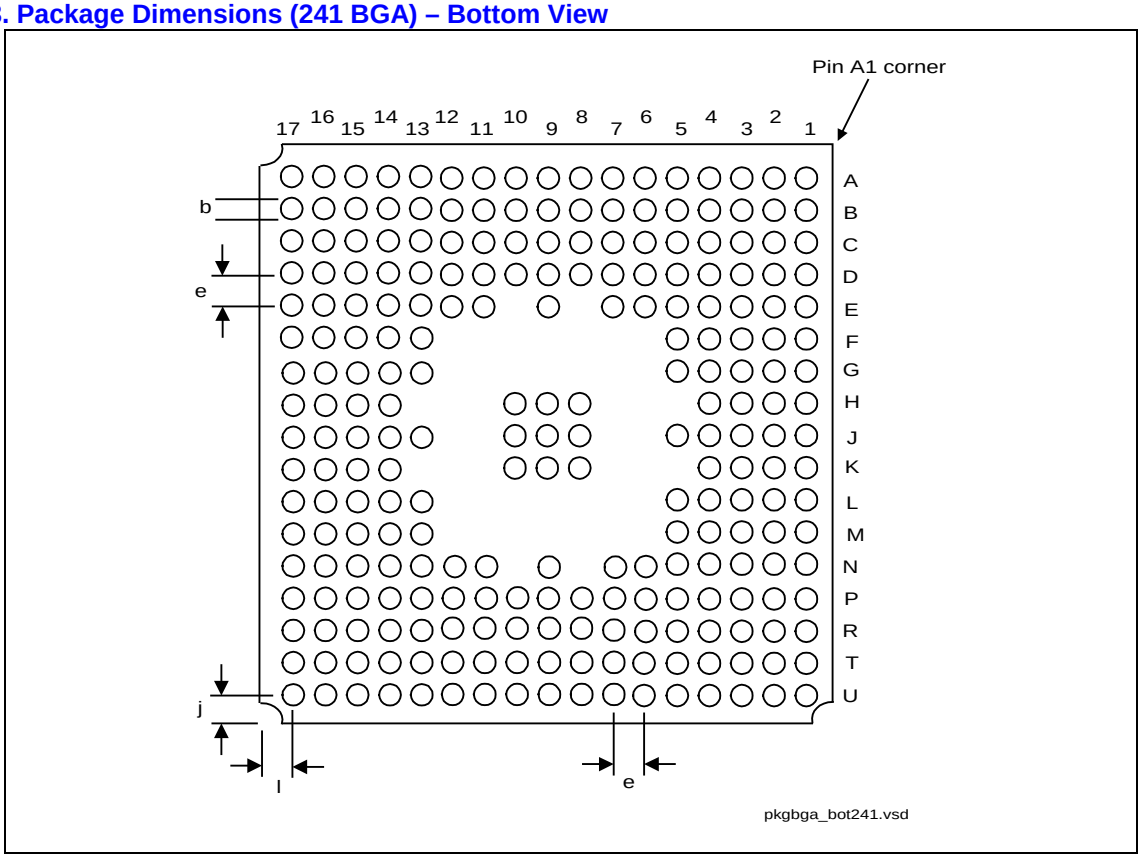


Table 11. BGA Package Dimensions (241 BGA)

Symbol	Min	Nominal	Max	Units	Note
A	2.19	2.38	2.57	mm	
A1	0.50	0.60	0.70	mm	
A2	1.12	1.17	1.22	mm	
D	22.80	23.00	23.20	mm	
D1	19.25	19.50	19.75	mm	
E	22.80	23.00	23.20	mm	
E1	19.25	19.50	19.75	mm	
e	1.27 (solder ball pitch)			mm	
l	1.34 REF.			mm	
J	1.34 REF.			mm	
M	17 x 17 Matrix			mm	
b^2	0.60	0.75	0.90	mm	
c	0.57	0.61	0.65	mm	

NOTES:

1. All dimensions and tolerances conform to ANSI Y14.5-1982
2. Dimension is measured at maximum solder ball diameter parallel to primary datum (-C-)
3. Primary Datum (-C-) and seating plane are defined by the spherical crowns of the solder balls.

5.3. MTH RSL Package Dimensions

Table 12. MTH RSL Package Dimensions

Signal	Ball on MTH	Package Dimension[1] (mils)	Signal	Ball on MTH	Package Dimension[1] (mils)
DQA0	A6	167.46	DQB7	A15	213.20
DQA1	C6	0.00	DQB8	C15	155.96
DQA2	A5	187.54	RQ0	A12	183.11
DQA3	C5	80.02	RQ1	C11	40.16
DQA4	B5	134.14	RQ2	A11	107.52
DQA5	C4	109.68	RQ3	C10	24.23
DQA6	A4	220.66	RQ4	B10	86.28
DQA7	C3	99.37	RQ5	A10	154.31
DQA8	A3	213.05	RQ6	A9	167.77
DQB0	C12	56.03	RQ7	C9	24.91
DQB1	B12	116.47			
DQB2	C13	78.24			
DQB3	A13	132.72	CFM	A7	105.81
DQB4	C14	117.82	CFM#	B7	120.73
DQB5	A14	159.52	CTM	B8	106.33
DQB6	B14	183.62	CTM#	A8	91.20

NOTES:
1. As described in latest *Intel® 820 Chipset Platform Design Guide*.
2. These package dimensions represent the trace length of the RSL signals in the MTH package. Note that these dimensions are normalized to 0 with DQA1 (the shortest trace on the MTH substrate). They do not represent actual lengths from pad to ball.

6. Testability

The 82805AA MTH supports the following test modes.

Number of Clocks[SCLKFDBK] TESTIN# Driven Low	Test Mode
<5	RESERVED. DO NOT ATTEMPT
6	All ‘Z’
7	Non-RAC NAND Chain
8-39	RESERVED. DO NOT ATTEMPT
40	RAC XOR Chain

6.1. Tri-state Mode

The Tri-state test mode is activated by asserting the TESTIN# signal low for 6 clocks[SCLKFDBK]. All outputs and bi-directional pins are tri-stated, including the NAND tree and XOR tree outputs.

6.2. NAND Tree Test Mode

6.2.1. SDRAM Interface Only

The 82805AA MTH has 3 NAND chains implemented for all non-RAC pins. This test mode activates by asserting the TESTIN# signal low for 7 clocks[SCLKFDBK]. This test mode can be used to check the connectivity of the pins.

Table 13. NAND CHAIN #1

Name	Ball	Chain Element #	Note
MD_63	E3	0	
MD_31	F3	1	
DQMIN	D1	2	
MD_62	E1	3	
MD_30	G4	4	
MD_60	G2	5	
MD_61	F1	6	
MD_28	H4	7	
MD_29	G1	8	
MD_59	G3	9	
MD_58	H2	10	
MD_26	H3	11	
MD_57	H1	12	
MD_27	J4	13	
MD_24	J2	14	
MD_56	J1	15	
MD_55	K1	16	
MD_22	K3	17	
MD_23	K2	18	
MD_53	L1	19	
MD_21	L2	20	
MD_25	K4	21	
MD_54	L3	22	
MD_20	L4	23	
MD_51	M1	24	
MD_52	M2	25	
MD_18	P1	26	
MD_16	N1	27	
CKE_1	N2	28	
MD_49	P2	29	
MD_19	M4	30	
SCLKB	R1	31	
CKE_3	N3	32	
MD_50	P3	33	
SCLKA	T1	34	
MD_17	N4	35	
DQM_7	T2	36	
CMD	A17		Output

Table 14. NAND CHAIN #2

Name	Ball	Chain Element #	Note
MD_48	R3	0	
CSAB_1	P4	1	
CSAB_2	R4	2	
CSBB_1	P5	3	
DQM_2	T3	4	
BAB_0	R5	5	
MAA_11	P6	6	
CSBB_2	T4	7	
CKE_0	T5	8	
DQM_6	U3	9	
BAA_0	R6	10	
DQM_3	U4	11	
BAB_1	T6	12	
CKE_2	U5	13	
BAA_1	U6	14	
MAB_11	P7	15	
MAA_7	P8	16	
MAB_12	T7	17	
MAA_12	U7	18	
MAA_9	T8	19	
MAA_8	R8	20	
MAA_10	U8	21	
MAB_10	U9	22	
MAB_7	P9	23	
MAB_9	T9	24	
MAB_8	R9	25	
MAA_4	U10	26	
MAA_5	T10	27	
MAB_4	U11	28	
MAA_2	T11	29	
MAA_6	P10	30	
MAA_3	U12	31	
MAB_5	R11	32	
MAB_6	P11	33	
MAB_2	T12	34	
MAB_3	U13	35	
CSBB_0	U14	36	
MAA_1	R12	37	
DQM_5	T14	38	

Name	Ball	Chain Element #	Note
RASBB	U15	39	
MAA_0	P12	40	
MAB_1	R13	41	
RASAB	U16	42	
CSBB_3	T15	43	
CSAB_3	T16	44	
DQM_4	R14	45	
DQM_0	R15	46	
MAB_0	P13	47	
SIO0	C16		Output

Table 15. NAND CHAIN #3

Name	Ball	Chain Element #	Note
WEAB	P14	0	
CASAB	P15	1	
MD_15	N14	2	
MD_13	M14	3	
CSAB_0	T17	4	
WEBB	P16	5	
MD_47	N15	6	
DQM_1	R17	7	
MD_14	N16	8	
CASBB	P17	9	
MD_46	N17	10	
MD_45	M16	11	
MD_12	L14	12	
MD_44	M17	13	
MD_11	L15	14	
MD_43	L16	15	
MD_42	L17	16	
MD_10	K15	17	
MD_9	K16	18	
MD_41	K17	19	
MD_8	J14	20	
MD_40	J16	21	
MD_39	J17	22	
MD_37	H17	23	
MD_38	H16	24	
MD_36	G17	25	
MD_7	H15	26	
MD_34	F17	27	
MD_6	H14	28	
MD_35	F16	29	
MD_4	G14	30	
MD_5	G15	31	
MD_32	E17	32	
MD_33	E16	33	
MD_3	F15	34	
MD_2	F14	35	
MD_1	E15	36	
SIO0	C16	37	
SCK	A16	38	
MD_0	E14	39	
SIO1	C17		Output

6.2.2. RAC Interface XOR Tree

The 82805AA MTH utilizes the following RAC XOR chain to check for connectivity on its Direct RDRAM channel. This test mode activates by asserting the TESTIN# signal low for 40 clocks (SCLKFDBK).

Table 16. RAC XOR Chain Mapping

ELEMENT Number	Associated Pin Number
0	DQA8
1	DQA7
2	DQA6
3	DQA5
4	DQA4
5	DQA3
6	DQA2
7	DQA1
8	DQA0
9	CTM
10	CTM#
11	CFM#
12	CFM
13	RQ6
14	RQ7
15	RQ5
16	RQ4
17	RQ3
18	RQ2
19	RQ1
20	RQ0
21	DQB1
22	DQB3
23	DQB0
24	DQB2
25	DQB5
26	DQB4
27	DQB6
28	DQB7
29	DQB8
	Output on CMD signal

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